

**ULDB TDRSS Interface Peer/Critical Design Review Action Items**  
**12/14/99**

No.	Date	Actionee	Status	Description/Response
1	11/3/99	D. Morgan	Closed 11/19/99	The panel recommends implementing independent monitoring lines on the TDI board instead of splicing wires for test point monitoring. It is also recommended to use separate drivers for the monitor lines. Investigate feasibility of this approach.  <i>No monitor test points will be brought out to the deck plate connector.</i>
2	11/3/99	D. Stuchlik	Open 11/19/99	Investigate whether or not bandwidth efficiency improvement is desirable by interleaving data on I and Q channels instead of combining data on the I and Q channels.
3	11/3/99	K. Ballou	Closed 11/19/99	Verify that FIFO buffers are flushed when unit is switched from PN mode to telemetry mode.  <i>Buffers will not be flushed automatically. Capability to flush buffers via command is available. This allows for flexibility in managing the buffers.</i>
4	11/3/99	D. Stuchlik	Closed 11/26/99	Determine total number of thermal cycle tests required, and under which configuration (i.e. stand alone or configured in system)  <i>Testing will include 10 thermal cycles. The test configuration will consist of two TDI boards in a single built up simulated flight computer.</i>
5	11/3/99	B. Mocarsky	Closed 11/19/99	Verify that actual flight RS-422 output cables will be used in testing.  <i>Actual flight cable will not be used. However, test cable will be non-shielded 22 AWG Teflon coated wire. The test cable is the same cable type as the flight cable.</i>
6	11/3/99	D. Stuchlik	Open 11/19/99	Investigate whether vacuum testing is required.
7	11/3/99	B. Mocarsky	Closed 11/19/99	Provide tentative date for completion of test plan.  <i>Tentative completion date is 11/30/99.</i>
8	11/3/99	D. Morgan	Closed 11/19/99	Determine what board status is required in housekeeping telemetry, in particular FIFO status  <i>The following items will be included in the housekeeping sampled at 1/minute:</i>

01/05/00

				<i>8-bit configuration register</i> <i>8-bit clock register</i> <i>8-bit latched FIFO status flag register</i>
9	11/3/99	K. Ballou	Open 12/10/99	Provide recommended algorithm or flowchart to flight software designers for optimum board operation.
10	11/3/99	D. Morgan	Open 11/19/99	Identify level of LDB testing required.
11	11/3/99	K. Ballou	Closed 11/19/99	Determine if ULDB/LDB mode selection will be selectable by a jumper or by flight software  <i>Mode selection will be selected via jumper</i>
12	11/3/99	K. Ballou	Closed 12/10/99	Provide board layout to thermal specialist.  <i>Layout has been provided.</i>
13	11/3/99	K. Ballou	Closed 11/30/99	Provide adequate diagrams and descriptions that identify all possible ULDB and LDB modes, and acquire approval from both programs.  <i>Information has been provided. See attachements.</i>

01/05/00